CLAIM AMENDMENTS:

The following listing replaces all previous versions of the claims:

1-15. (Cancelled)

16. (New) A semiconductor device, comprising:

a solid state device having a surface and an external connection surface which is a surface on a side opposite the surface,

a semiconductor chip having a functional surface,

a connecting member provided between the surface of the solid state device and the functional surface of the semiconductor chip, the connecting member extending over a distance between the surface of the solid state device and the functional surface of the semiconductor chip and having a constant width,

an insulating film provided on the surface of the solid state device, the insulating film having an opening greater in size than the semiconductor chip, and

a sealing layer that completely seals the opening and a space between the solid state device and the semiconductor chip.

17. (New) The semiconductor device according to claim 16, wherein a connection pad is provided on the surface of the solid state device.

18. (New) The semiconductor device according to claim 17, wherein the connecting member includes the connection pad.

19. (New) The semiconductor device according to claim 17, wherein the solid state device and the semiconductor chip are bonded by means of the connecting member including the connection pad with a predetermined interval between the solid state device and the semiconductor chip.

20. (New) The semiconductor device according to claim 16, wherein the solid state device and the semiconductor chip are electrically connected together.

21. (New) The semiconductor device according to claim 16, wherein the insulating film is a solder resist film.

22. (New) The semiconductor device according to claim 16, wherein the insulating film has a thickness smaller than an interval between the surface of the solid state device and the semiconductor chip.

23. (New) The semiconductor device according to claim 16, wherein the opening of the insulating film is formed so that the semiconductor chip completely falls laterally within the opening.

24. (New) The semiconductor device according to claim 16, wherein a lateral distance between an outer periphery of the semiconductor chip and an edge of the opening of the insulating film is 0.1 mm or more.

25. (New) The semiconductor device according to claim 16,

wherein the sealing layer is provided in such a manner as to fill the opening with the sealing layer, and

wherein the sealing layer serves to seal a gap between the solid state device and the semiconductor chip and to protect the functional surface, the connecting member and an exposed part of the surface of the solid state device exposed from the opening of the insulating film.

26. (New) The semiconductor device according to claim 16, wherein an end electrode that is electrically connected to the connecting member is formed at an end of the solid state device.

27. (New) The semiconductor device according to claim 26, wherein the end electrode leads from the surface to the external connection surface via an end face on the solid state device.

28. (New) The semiconductor device according to claim 26, wherein the semiconductor device can establish an electric connection with other wiring board in the end electrode.

29. (New) The semiconductor device according to claim 16, wherein the semiconductor chip includes two or more semiconductor chips each connected to the solid state device in a flip chip manner.

30. (New) The semiconductor device according to claim 29, wherein the opening of the insulating film includes two or more openings each completely laterally including each semiconductor chip.

31. (New) The semiconductor device according to claim 16, wherein the semiconductor chip has the functional surface only on one surface of the semiconductor chip.

32. (New) The semiconductor device according to claim 16, wherein the functional surface is formed not entirely on one surface of the semiconductor chip.

33. (New) The semiconductor device according to claim 16, wherein the sealing layer is not on the insulating film.

34. (New) The semiconductor device according to claim 16, wherein the sealing layer at least partially covers a side surface of the semiconductor chip.

35. (New) The semiconductor device according to claim 34, wherein the sealing layer does not reach an upper surface of the semiconductor chip.

36. (New) The semiconductor device according to claim 35, wherein the sealing layer is not on the insulating film.

37. (New) The semiconductor device according to claim 16, wherein no other wiring than a connection pad for connection with the semiconductor chip is provided on the solid state device in the opening of the insulating film.

38. (New) A semiconductor device, comprising:

a solid state device having a surface and an external connection surface which is a surface on a side opposite the surface,

a semiconductor chip having a functional surface,

a connecting member provided between the surface of the solid state device and the functional surface of the semiconductor chip, the connecting member having a constant width,

an insulating film provided on the surface of the solid state device, the insulating film having an opening greater in size than the semiconductor chip, and

a sealing layer that completely seals the opening and a space between the solid state device and the semiconductor chip,

wherein no level difference, other than a level difference in the sealing layer or a level difference formed by a wiring connected to the connecting member via a connection pad provided on the surface of the solid state device, exists within the opening of the insulating film.

39. (New) The semiconductor device according to claim 38, wherein a connection pad is provided on the surface of the solid state device.

40. (New) The semiconductor device according to claim 39, wherein a width of the connection pad is equal to a width of the connecting member.

41. (New) The semiconductor device according to claim 39, wherein the solid state device and the semiconductor chip are bonded by means of the connecting member connected to the connection pad with a predetermined interval between the solid state device and the semiconductor chip.

42. (New) The semiconductor device according to claim 38, wherein the solid state device and the semiconductor chip are electrically connected together.

43. (New) The semiconductor device according to claim 38, wherein the insulating film is a solder resist film.

44. (New) The semiconductor device according to claim 38, wherein the insulating film has a thickness smaller than an interval between the surface of the solid state device and the semiconductor chip.

45. (New) The semiconductor device according to claim 38, wherein the opening of the insulating film is formed so that the semiconductor chip completely falls laterally within the opening.

46. (New) The semiconductor device according to claim 38, wherein a lateral distance between an outer periphery of the semiconductor chip and an edge of the opening of the insulating film is 0.1 mm or more.

47. (New) The semiconductor device according to claim 38,

wherein the sealing layer is provided in such a manner as to fill the opening with the sealing layer, and

wherein the sealing layer serves to seal a gap between the solid state device and the semiconductor chip and to protect the functional surface, the connecting member and an exposed part of the surface of the solid state device exposed from the opening of the insulating film.

48. (New) The semiconductor device according to claim 38, wherein an end electrode that is electrically connected to the connecting member is formed at an end of the solid state device.

49. (New) The semiconductor device according to claim 48, wherein the end electrode leads from the surface to the external connection surface via an end face on the solid state device.

50. (New) The semiconductor device according to claim 48, wherein the semiconductor device can establish an electric connection with other wiring board in the end electrode.

51. (New) The semiconductor device according to claim 38, wherein the semiconductor chip includes two or more semiconductor chips each connected to the solid state device in a flip chip manner.

52. (New) The semiconductor device according to claim 51, wherein the opening of the insulating film includes two or more openings each completely laterally including each semiconductor chip.

53. (New) The semiconductor device according to claim 38, wherein the semiconductor chip has the functional surface only on one surface of the semiconductor chip.

54. (New) The semiconductor device according to claim 38, wherein the functional surface is formed not entirely on one surface of the semiconductor chip.

55. (New) The semiconductor device according to claim 38, wherein the sealing layer is not on the insulating film.

56. (New) The semiconductor device according to claim 38, wherein the sealing layer at least partially covers a side surface of the semiconductor chip.

57. (New) The semiconductor device according to claim 56, wherein the sealing layer does not reach an upper surface of the semiconductor chip.

58. (New) The semiconductor device according to claim 57, wherein the sealing layer is not on the insulating film.

59. (New) The semiconductor device according to claim 38, wherein no other wiring than a connection pad for connection with the semiconductor chip is provided on the surface of the solid state device in the opening of the insulating film.

60. (New) The semiconductor device according to claim 38, wherein the insulating film has no opening in which an insulative film is exposed.

61. (New) A semiconductor device, comprising:

a solid state device having a surface and an external connection surface which is a surface on a side opposite the surface,

a metallic ball provided on the external connection surface,

a semiconductor chip having a functional surface,

a connecting member provided between the surface of the solid state device and the functional surface of the semiconductor chip, the connecting member extending over a distance between the surface of the solid state device and the functional surface of the semiconductor chip and having a constant width,

an insulating film provided on the surface of the solid state device, the insulating film having an opening greater in size than the semiconductor chip, and

a sealing layer that completely seals the opening and a space between the solid state device and the semiconductor chip.

62. (New) The semiconductor device according to claim 61, wherein the metallic ball is re-wired inside the solid state device and/or on the surface of the solid state device, and is electrically connected to the connecting member on a side of the surface.

63. (New) The semiconductor device according to claim 61, wherein the semiconductor chip can be bonded with other wiring board via the metallic ball.

64. (New) The semiconductor device according to claim 61, wherein a connection pad is provided on the surface of the solid state device.

65. (New) The semiconductor device according to claim 62, wherein the connecting member includes the connection pad.

66. (New) The semiconductor device according to claim 62, wherein the solid state device and the semiconductor chip are bonded by means of the connecting member including the connection pad with a predetermined interval between the solid state device and the semiconductor chip.

67. (New) The semiconductor device according to claim 61, wherein the solid state device and the semiconductor chip are electrically connected together.

68. (New) The semiconductor device according to claim 61, wherein the insulating film is a solder resist film.

69. (New) The semiconductor device according to claim 61, wherein the insulating film has a thickness smaller than an interval between the surface of the solid state device and the semiconductor chip.

70. (New) The semiconductor device according to claim 61, wherein the opening of the insulating film is formed so that the semiconductor chip completely falls laterally within the opening.

71. (New) The semiconductor device according to claim 61, wherein a lateral distance between an outer periphery of the semiconductor chip and an edge of the opening of the insulating film is 0.1 mm or more.

72. (New) The semiconductor device according to claim 61,

wherein the sealing layer is provided in such a manner as to fill the opening with the sealing layer, and

wherein the sealing layer serves to seal a gap between the solid state device and the semiconductor chip and to protect the functional surface, the connecting member and an exposed part of the surface of the solid state device exposed from the opening of the insulating film.

73. (New) The semiconductor device according to claim 61, wherein the semiconductor chip includes two or more semiconductor chips each connected to the solid state device.

74. (New) The semiconductor device according to claim 73, wherein the opening of the insulating film includes two or more openings each completely laterally including each semiconductor chip.

75. (New) The semiconductor device according to claim 61, wherein the semiconductor chip has the functional surface only on one surface of the semiconductor chip.

76. (New) The semiconductor device according to claim 61, wherein the functional surface is formed not entirely on one surface of the semiconductor chip.

77. (New) The semiconductor device according to claim 61, wherein the sealing layer is not on the insulating film.

78. (New) The semiconductor device according to claim 61, wherein the sealing layer at least partially covers a side surface of the semiconductor chip.

79. (New) The semiconductor device according to claim 78, wherein the sealing layer does not reach an upper surface of the semiconductor chip.

80. (New) The semiconductor device according to claim 79, wherein the sealing layer is not on the insulating film.

81. (New) The semiconductor device according to claim 61, wherein no other wiring than a connection pad for connection with the semiconductor chip is provided on the solid state device in the opening of the insulating film.

82. (New) A semiconductor device, comprising:

a solid state device having a surface and an external connection surface which is a surface on a side opposite the surface,

a metallic ball provided on the external connection surface,

a semiconductor chip having a functional surface,

a connecting member provided between the surface of the solid state device and the functional surface of the semiconductor chip, the connecting member having a constant width,

an insulating film provided on the surface of the solid state device, the insulating film having an opening greater in size than the semiconductor chip, and

a sealing layer that completely seals the opening and a space between the solid state device and the semiconductor chip,

wherein no level difference, other than a level difference in the sealing layer, exists within the opening of the insulating film.

83. (New) The semiconductor device according to claim 82, wherein the metallic ball is re-wired inside the solid state device, and is electrically connected to the connecting member on a side of the surface.

84. (New) The semiconductor device according to claim 82, wherein the semiconductor chip can be bonded with other wiring board via the metallic ball.

85. (New) The semiconductor device according to claim 82, wherein a connection pad is provided on the surface of the solid state device.

86. (New) The semiconductor device according to claim 85, wherein a width of the connection pad is equal to a width of the connecting member.

87. (New) The semiconductor device according to claim 85, wherein the solid state device and the semiconductor chip are bonded by means of the connecting member connected to the connection pad with a predetermined interval between the solid state device and the semiconductor chip.

88. (New) The semiconductor device according to claim 82, wherein the solid state device and the semiconductor chip are electrically connected together.

89. (New) The semiconductor device according to claim 82, wherein the insulating film is a solder resist film.

90. (New) The semiconductor device according to claim 82, wherein the insulating film has a thickness smaller than an interval between the surface of the solid state device and the semiconductor chip.

91. (New) The semiconductor device according to claim 82, wherein the opening of the insulating film is formed so that the semiconductor chip completely falls laterally within the opening.

92. (New) The semiconductor device according to claim 82, wherein a lateral distance between an outer periphery of the semiconductor chip and an edge of the opening of the insulating film is 0.1 mm or more.

93. (New) The semiconductor device according to claim 82,

wherein the sealing layer is provided in such a manner as to fill the opening with the sealing layer, and

wherein the sealing layer serves to seal a gap between the solid state device and the semiconductor chip and to protect the functional surface, the connecting member and an exposed part of the surface of the solid state device exposed from the opening of the insulating film.

94. (New) The semiconductor device according to claim 82, wherein the semiconductor chip includes two or more semiconductor chips each connected to the solid state device.

95. (New) The semiconductor device according to claim 94, wherein the opening of the insulating film includes two or more openings each completely laterally including each semiconductor chip.

96. (New) The semiconductor device according to claim 82, wherein the semiconductor chip has the functional surface only on one surface of the semiconductor chip.

97. (New) The semiconductor device according to claim 82, wherein the functional surface is formed not entirely on one surface of the semiconductor chip.

98. (New) The semiconductor device according to claim 82, wherein the sealing layer is not on the insulating film.

99. (New) The semiconductor device according to claim 82, wherein the sealing layer at least partially covers a side surface of the semiconductor chip.

100. (New) The semiconductor device according to claim 99, wherein the sealing layer does not reach an upper surface of the semiconductor chip.

101. (New) The semiconductor device according to claim 100, wherein the sealing layer is not on the insulating film.

102. (New) The semiconductor device according to claim 82, wherein no other wiring than a connection pad for connection with the semiconductor chip is provided on the solid state device in the opening of the insulating film.